Exhibit 8

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Assistant Commissioner for Patents
Washington, D.C. 20231
On November 4, 1999
By: Jennifer Lees

Attorney Docket No.: 18865-P
Client Reference No.: 17732/722

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Brian Sze-Ki Mo et al.

Application No.: 08/970,221

Filed: November 14, 1997

For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE

Examiner: Tran, H.

Art Unit: 2815

AMENDMENT

#15B
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Nov 17, 99

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed August 4, 1999, please amend the above-identified application as follows:

IN THE CLAIMS:

Applicants hereby cancel non-elected claims 23-45. With respect to the remaining claims, please amend claims 1, 7-8, 14, 18-19 and 22, cancel claims 3-4 and add new claims 46-52 as set forth below. For convenient reference, all pending claims are reproduced below with unamended claims appearing in smaller font.

1. (Once Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, **[the deepest portion of]** said heavy body extending **[less deeply]** into said **[semiconductor substrate]** doped well to a depth that is less than said **[predetermined]** depth of said **[trench]** doped well, **[; and**

a doped well surrounding the heavy body beneath the heavy body]

wherein, the depth of said doped heavy body is controlled so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. Canceled.

4. Canceled.

5. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

6. The trenched field effect transistor of claim 1 wherein there is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field when voltage is applied to the transistor to occur in the area of the interface.

7. (Once Amended) The trenched field effect transistor of claim 6 wherein said **[abrupt junction has a sheet resistance profile substantially as shown in Fig. 5]** doped heavy body has a first dopant concentration near the doped heavy body interface, and a second dopant concentration that is less than the first dopant concentration near its upper surface.

8. (Once Amended) An array of transistor cells comprising:

a semiconductor substrate;

a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches;

surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench;

a doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

[positioned between each pair of gate-forming trenches,] a doped heavy body formed inside the doped well and positioned adjacent each source junction, the deepest portion of **[each]** said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

[a doped well surrounding each heavy body beneath the heavy body;

and p+ and n+] alternating heavy body and source contact**[s]** regions **[disposed]** defined at the surface of the semiconductor substrate **[and arranged in alternation]** along the length of the contact area.

9. The array of transistor cells of claim 8, wherein each said doped well has a substantially flat bottom.

10. The array of transistor cells of claim 8 wherein the depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field when voltage is applied to the transistor will occur approximately halfway between adjacent gate-forming trenches.

11. The array of transistor cells of claim 8 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

12. The array of transistor cells of claim 8 wherein each said gate-forming trench has rounded top and bottom corners.

13. The array of transistor cells of claim 8 wherein there is an abrupt junction at each interface between the heavy body and the well, to cause the peak electric field when voltage is applied to the transistor to occur in the area of the interface.

14. (Once Amended) The array of transistor cells of claim [8] 9 further comprising a field termination structure surrounding the periphery of the array.

15. The array of transistor cells of claim 14 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

16. The array of transistor cells of claim 14 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

17. The array of transistor cells of claim 16 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

18. (Once Amended) A semiconductor die comprising:

a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same;

a doped well formed in the semiconductor substrate between each pair of gate-forming trenches within which source junctions are formed, said doped well extending to a depth that is less than said predetermined depth of said gate-forming trench; and

surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said **[predetermined]** depth of said **[gate-forming trenches]** doped well.

19. (Once Amended) The semiconductor die of claim 18 wherein said field termination structure comprises a deep doped well.

20. The semiconductor die of claim 18 wherein said field termination structure comprises a termination trench.

21. The semiconductor die of claim 20 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

22. (Once Amended) The semiconductor die of claim 18 wherein each of said DMOS transistor cells further comprises a doped heavy body **[and said doped heavy body extends]** extending into said **[semiconductor substrate]** doped well to a depth that is less than the **[predetermined]** depth of said **[gate-forming trenches]** doped well.

~~23~~ -- ~~46~~. (New) The array of transistor cells of claim ~~8~~ wherein the doped heavy body forms a continuous doped region along substantially the entire length of said contact area.

47. (New) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth;

wherein, the doped heavy body forms a continuous doped region along substantially the entire longitudinal axis of a trench.

~~48~~. (New) The trenched field effect transistor of claim ~~47~~ further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

~~49~~. (New) The trenched field effect transistor of claim ~~48~~ wherein the contact areas alternate between source and heavy body contacts.

50. (New) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well,

wherein, the controlled depth of the doped heavy body eliminates the need for additional epitaxial layer.

51. (New) The trenched field effect transistor of claim 6 wherein said doped heavy body is formed by a double implant of said dopant of the second conductivity type.

52. (New) The trenched field effect transistor of claim 51 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

REMARKS

Upon entry of this amendment which amends claims 1, 7-8, 14, 18-19, 22, cancels claim 3, and adds new claims 46-52, claims 1-2, 4-22 and 46-52 would remain pending. Previously examined claims 7 and 8 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite, claims 1-2, 4-6, 8-13, 15, and 17-22 were rejected under 35 U.S.C. §102(b) as being anticipated by USPN 5,689,128 to Hshieh et al. (hereinafter "Hshieh '128"), and claims 3, 10, 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hshieh '128 in view of known prior art. Reconsideration of the pending claims in view of the above amendments and the comments below is respectfully requested.

The Rejections

- Section 112

Claims 7 and 8 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for "[failing] to point out what is included or excluded by the claim language." Specifically, claim 7 has been rejected as being "an omnibus claim." Claim 7

has been amended to delete any reference to the figures. As amended, claim 7 expressly defines the sheet resistance profile of the heavy body junction. Amended claim 7 is supported by the profile depicted in Figure 5 which is further described at page 12, lines 5-9 of the specification.

In rejecting claim 8, the Examiner states that "It is unclear how the a doped well surrounding the heavy body beneath the heavy body." The rejection further asserts that "the examiner's interpretation of the claim limitation is a doped well structure located below the heavy body." Applicants agree with the Examiner's interpretation in that to the extent the heavy body is formed inside the doped well, the doped well would be below the heavy body. The doped well, however, does surround the heavy body as well. To better define this structure, claim 8 has been amended to remove the "surrounding .. beneath" language and to define the doped heavy body as being "formed inside the doped well."

It is submitted that claims 7 and 8 as amended clearly point out and distinctly claim the invention. Accordingly, withdrawal of this rejection is respectfully requested.

- Section 102(b): Hshieh '128

Claims 1-2, 4-6, 8-13, 15, and 17-22 have been rejected under 35 U.S.C. §102(b) as being anticipated by Hshieh '128. The rejection asserts that all of the elements of the rejected claims are disclosed by Hshieh '128. It is submitted that Hshieh '128 fails to teach or suggest a number of the claimed elements and various combinations thereof as explained below.

With respect to claim 1, the rejection states that Hshieh '128 shows "a semiconductor substrate 10", "a pair of doped source junctions 20", "a doped heavy body 34" and "a doped well." It is respectfully submitted that the rejection mischaracterizes the structure disclosed by Hshieh '128. Hshieh '128 defines region 34 as "a second (upper) epitaxial layer." [Hshieh '128, col. 3, line 66]. As also indicated in Figure 2 (or 3) of Hshieh '128, epitaxial layer 34 has the same dopant type (n) as the first epitaxial layer 12 and the substrate 10. Epitaxial layer 34 therefore cannot be characterized as a doped heavy body.

Claim 1 has been amended to recite dopant types for the various regions of the claimed device in order to further clarify their structural relationship. As amended, the claimed substrate and source junctions have dopants of a "first conductivity type" while the "doped heavy body" and the "doped well" have "dopants of the second conductivity type" that is "opposite to the first conductivity type." Therefore, epitaxial layer 34 of Hshieh '128 that is n-type (the same polarity as the doping of the substrate 10 and the source regions 20) cannot be characterized as the claimed "doped heavy body" that has "dopants of the second conductivity type" opposite to that of the substrate.

In fact, there is no structure in the Hshieh '128 device that discloses or even suggests the claimed "doped heavy body" and its combination with the other claimed elements. Figure 1 of Hshieh '128 shows a "P+ doped body contact region 18", a "P doped body region 14", and "a P+ deep body region 16." [Hshieh '128, col. 3, lines 14-20, and lines 37-40]. However, none of these regions can be characterized as the claimed "doped heavy body." Hshieh's "P+ doped body contact region 18" is just that, a contact region. That is, the sole purpose of the "P+ doped body contact region 18" is "to promote electrical contact between the body region 14 and the overlying source-body metallization 30." [Hshieh '128, col. 3, lines 38-40]. Hshieh's contact region 18 is therefore relatively shallow and is not intended to impact the location of "the peak electric field" that may cause destructive breakdown when voltage is applied to the transistor. Amended claim 1, in contrast, defines the "doped heavy body" as having a depth that "is controlled so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench ...." Hshieh's contact region 18, thus, neither teaches nor suggests the claimed "doped heavy body."

Hshieh '128 is, in fact, concerned with avoiding "destructive breakdown at the bottom of the trenches, due to the higher electric field ...." [Hshieh '128, col. 4, lines 22-24, also see, col. 1, lines 25-34, and col. 2, lines 15-18]. However, Hshieh '128 discloses structures that are fundamentally different than that of the claimed invention. In the first embodiment shown in Figure 1 of Hshieh '128, for example, Hshieh '128 teaches using a

"P+ deep body region 16" that "extends 0.5 μm below the bottom of the trench." [Hshieh '128, col. 3, lines 26-27, underline added]. The effect of this "deep" body region is such that "the avalanche breakdown occurs from the lowest portion of this P+ deep body region into the underlying drain region." [Hshieh '128, col. 1, lines 25-34]. This helps distinguish amended claim 1 from Hshieh '128 in two respects. First, the need for the "P+ deep body region 16" makes clear that contact region 18 cannot be characterized as the claimed "doped heavy body" whose "depth is controlled so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench ...." Second, as clearly recited by amended claim 1, the claimed heavy body "[extends] into said doped well to a depth that is less than said depth of said doped well", and the doped well has a "depth that is less than said predetermined depth of the trench." Therefore, contrary to the teachings of Hshieh '128, the transistor of claim 1 does not include a "deep" body that "extends 0.5 μm below the bottom of the trench."

Hshieh '128 does disclose alternative embodiments in Figures 2 and 3 wherein there is no P+ region that extends below the bottom of the trench. However, claim 1 is still distinguished from both of those embodiments for a number of reasons. In Figure 2, Hshieh '128 includes a "P+ deep body region 36 which does not extend as deep as the bottom of the trenches ...." [Hshieh '128, col. 4, lines 2-3]. As clearly depicted in Figure 2, however, "P+ deep body region 36" is deeper than the "P doped body region 14." That is, unlike the claimed heavy body (e.g., region 34 in Figs. 1A and 1B of the instant application) which is shallower than the well region (36), Hshieh '128 teaches in Figure 2 to extend the depth of "P+ deep body region 36" below the depth of P doped body region 14. Amended claim 1 which defines the "heavy body extending into said doped well to a depth that is less than said depth of said doped well" is therefore clearly distinguished from the Hshieh '128 figure 2 embodiment.

With respect to the embodiment shown in Figure 3 of Hshieh '128, this embodiment completely does away with the "P+ deep body region." [Hshieh '128, col. 4, lines 14-16]. Hshieh '128 does state that "The intention is that there be avalanche breakdown

where the P+ body contact 20 approaches the underlying drift region." But, this statement is immediately followed by, "Otherwise the dimensions and parameters of the FIG. 3 transistor are similar to those of FIG. 2" [Hshieh '128, col. 4, lines 27-31]. In other words, for the transistor shown in Figure 3, Hshieh '128 does not contemplate varying the "P+ doped body contact region" in its dimensions or parameters to impact the location where the peak electric field occurs when voltage is applied to the transistor. This is in contrast to the claimed invention as set out in amended claim 1 wherein it is recited that "the depth of the doped heavy is controlled so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench." Hshieh '128 very clearly does not contemplate such a combination as it expressly teaches at column 4, lines 20-23, that "the FIG. 3 transistor may have some residual problem of oxide rupture, i.e., destructive breakdown at the bottom of the trenches, due to the higher electric field ...." Hshieh '128 further teaches that "the embodiment of FIG. 2 is likely to perform better in typical applications than the embodiment of FIG. 3." [Hshieh '128, col. 4, lines 18-20]. By thus favoring an embodiment that uses a "P+ deep body" along with a "double epitaxial layer structure" (first epitaxial layer 12 and second (upper) expitaxial layer 34), Hshieh '128 teaches away from the claimed invention. Accordingly, claim 1 as amended is neither disclosed nor suggested by Hshieh '128.

Claims 2, 5-7, and newly added claims 50-52 ultimately depend from claim 1 and thus derive patentability therefrom. These claims, however, recite additional novel and non-obvious features that further distinguish over the cite reference. Claim 7, for example, defines a specific dopant concentration profile for the doped heavy body that is neither disclosed nor suggested by Hshieh '128. Similarly, no where in Hshieh '128 could there be found any reference to or suggestion of forming the doped heavy body by "a double implant of said dopant of the second conductivity type" as set forth in claim 51, let alone one that specifies the relative energy levels of the implants as set forth in claim 52. Both of these new claims 51 and 52 are supported by the specification by the paragraph bridging pages 11 and 12. Yet further, newly added claim 50 recites a structure wherein an "epitaxial layer ...[is] formed between the substrate and the doped well" and wherein "the controlled depth of the doped heavy body eliminates the need for additional epitaxial layer." This is also clearly

distinguished from the main embodiment of the Hshieh '128 reference wherein the use of two epitaxial layers (12 and 34) are taught. Thus, claims 2, 5-7 and 50-52 are clearly patentable over the cited reference.

With respect to independent claim 8, the rejection cites Hshieh '128 as disclosing all the various elements. However, it is not made clear how, and where in Hshieh '128 there is teaching of the various elements. For example, claim 8 recites "a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction." This is shown diagrammatically in Figure 1 of the instant application where trenches 14 extend in parallel in a stripped fashion or in what is commonly referred to as "open cell" structure. No where in Hshieh '128 could there be found any reference to this type of claimed structure. The closest Hshieh '128 comes to defining an array is at column 2, lines 45 et seq., where it is stated, "It is to be understood that this cross-section is drawn conventionally showing a portion of several cells of a typical transistor which may include thousands of such cells." There is, however, no indication of how these cells are arranged. The cross-sectional views shown in Figures 1-3 of Hshieh '128 could well be part of a structure that is commonly referred to as "closed cell" array where the trench cells have hexagonal structure as opposed to a striped one. Therefore, Hshieh '128 does not disclose this element of the claim.

Claim 8 further recites "a doped heavy body formed inside the doped well." As extensively discussed above, Hshieh '128 clearly fails to teach or suggest the use of a "doped heavy body" as claimed. Nor does the rejection identify which element of Hshieh's device corresponds to the claimed "doped heavy body." Yet further, claim 8, as amended, recites "alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area." Again, the rejection is silent as to how Hshieh '128 anticipates this element. This is so because Hshieh '128 neither discloses nor suggests any structure even remotely similar to the claimed "alternating heavy body and source contact regions." Amended claim 8 is thus clearly distinguished over the cited reference in at least these several respects.

Claims 9-17 ultimately depend from claim 8 and therefore derive patentability therefrom. These claims, however, recite additional novel and non-obvious feature that further distinguish over the cited reference. For example, claim 15 recites "a field termination structure [comprising] a well having a depth greater than that of the gate-forming trenches." Hshieh '128, nor any of the other cited references, disclose or suggest such a termination structure. These claims are therefore patentable over the cited references.

As for claim 18, this claim has been amended to clearly recite a termination structure for a trench DMOS transistor that is novel and non-obvious over any of the references of record. Except for a brief reference to the general use of known termination structures at column 3, lines 43-49, Hshieh '128 does not disclose any specific termination structure, let alone one that has the specific structural characteristics set forth in claim 18. Hshieh et al. do describe a particular termination structure in another U.S. Patent Number 5,578,851 (hereinafter Hshieh '851) which was cited in an information disclosure statement filed March 9, 1998. The termination structure in Hshieh '851, however, is substantially different than that set forth in amended claim 18. Specifically, Hshieh '851 teaches forming "P+ field rings (termination structures) 110, 112, 114" that are "similar" in dimension to "P+ deep body regions 106, 108." [Hshieh '851, col. 2, lines 60-67]. That is, as shown in all of the various figures, Hshieh '851 teaches forming the P+ termination wells (110, 12, 114) at the same time as the P+ deep body regions (106, 108) so that they have identical characteristics, including junction depth. [Hshieh '851, col. 4, lines 22-24]. Amended claim 18, however, specifically recites "a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said depth of said doped well." Therefore, Hshieh '851 termination structure clearly does not disclose the claimed termination structure. Nor can be argued that Hshieh '851 suggests the claimed structure as the termination structure of claim 18 requires separate processing steps to form the "doped well" and the "deeper" termination well. Claim 18 is therefore clearly patentable over the cited references. Claims 19-22 depend from claim 18 and derive patentability therefrom. Applicants respectfully request the withdrawal of the rejection with respect to these claims.

New Claims New Claims:

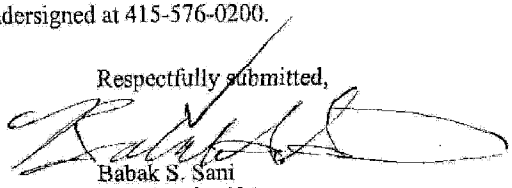
Claims 47-49 have been added to claim an aspect of the present invention that was not adequately claimed by the application as originally filed. Claim 47 is primarily directed to a trench transistor with a "doped heavy body [formed as] a continuous doped region along substantially the entire longitudinal axis of a trench." This aspect of the invention is depicted in, for example, Figures 4H, 4I and 4J, wherein, a P+ heavy body region is shown as a continuous junction along the longitudinal axis of each trench. No teaching or suggestion of such a structure could be found in any of the cited references. It is respectfully submitted that claim 47 and its dependent claims 48-49 are patentable over the cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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